



# Design Challenges and Considerations of Wolfspeed 22kW High Efficiency Bi-directional DCDC Converter

Power Applications  
Oct. 2020

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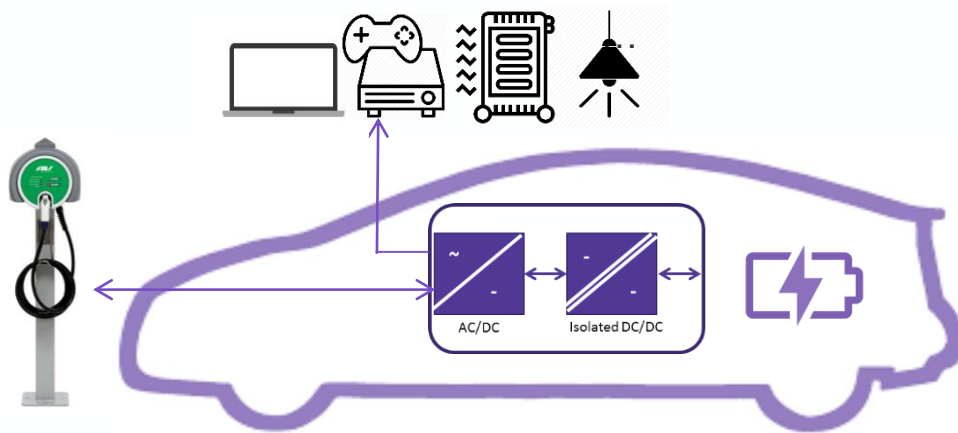
- Specifications and Design Challenges
- Topology Selection
- Power Components Selection
- Key Magnetics
- Control of the CLLC Converter
- Gate Driver and Bias Power Supply
- PCB Layout Considerations
- Test Results

# Specifications and Design Challenges

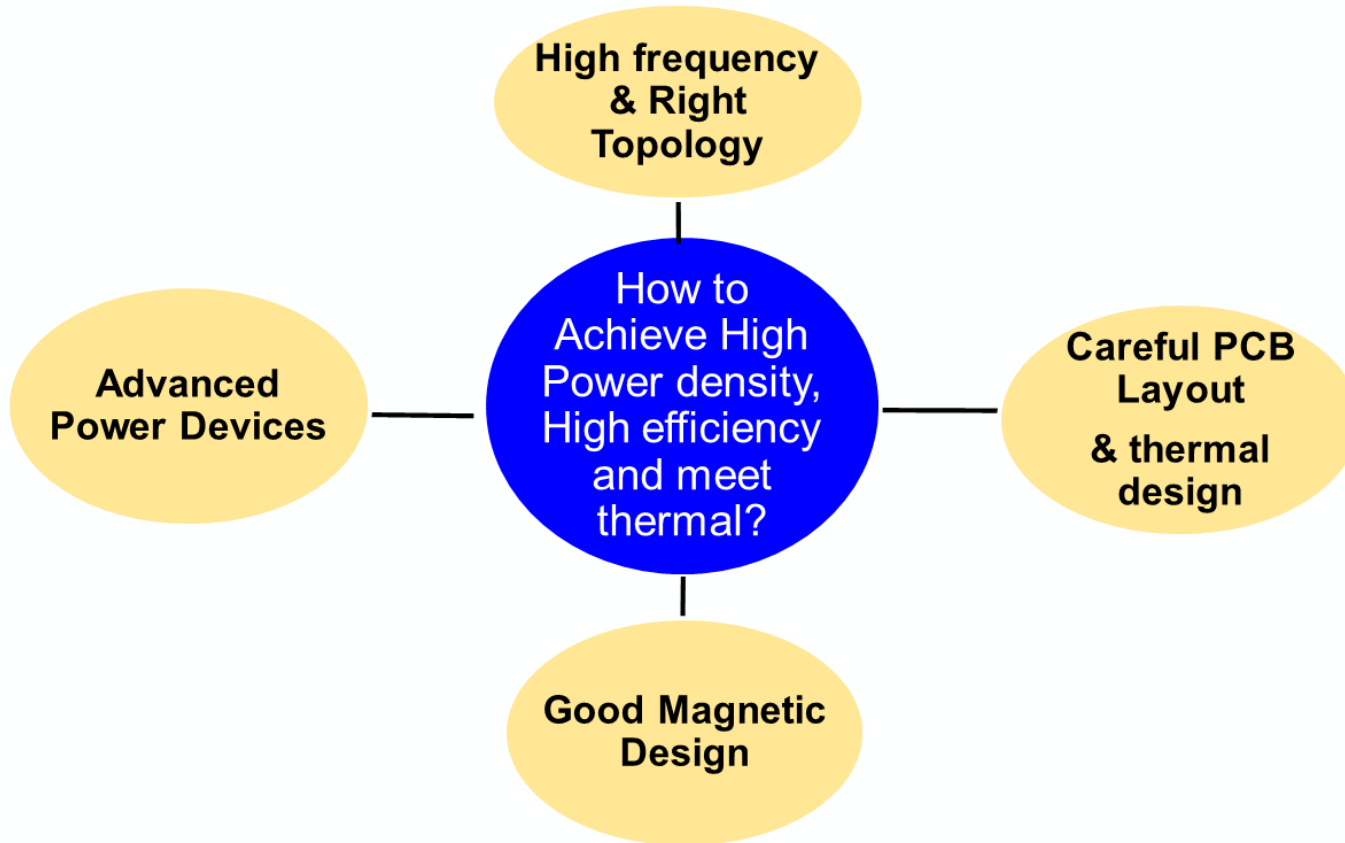
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# 22kW Bi-Directional OBC Specifications

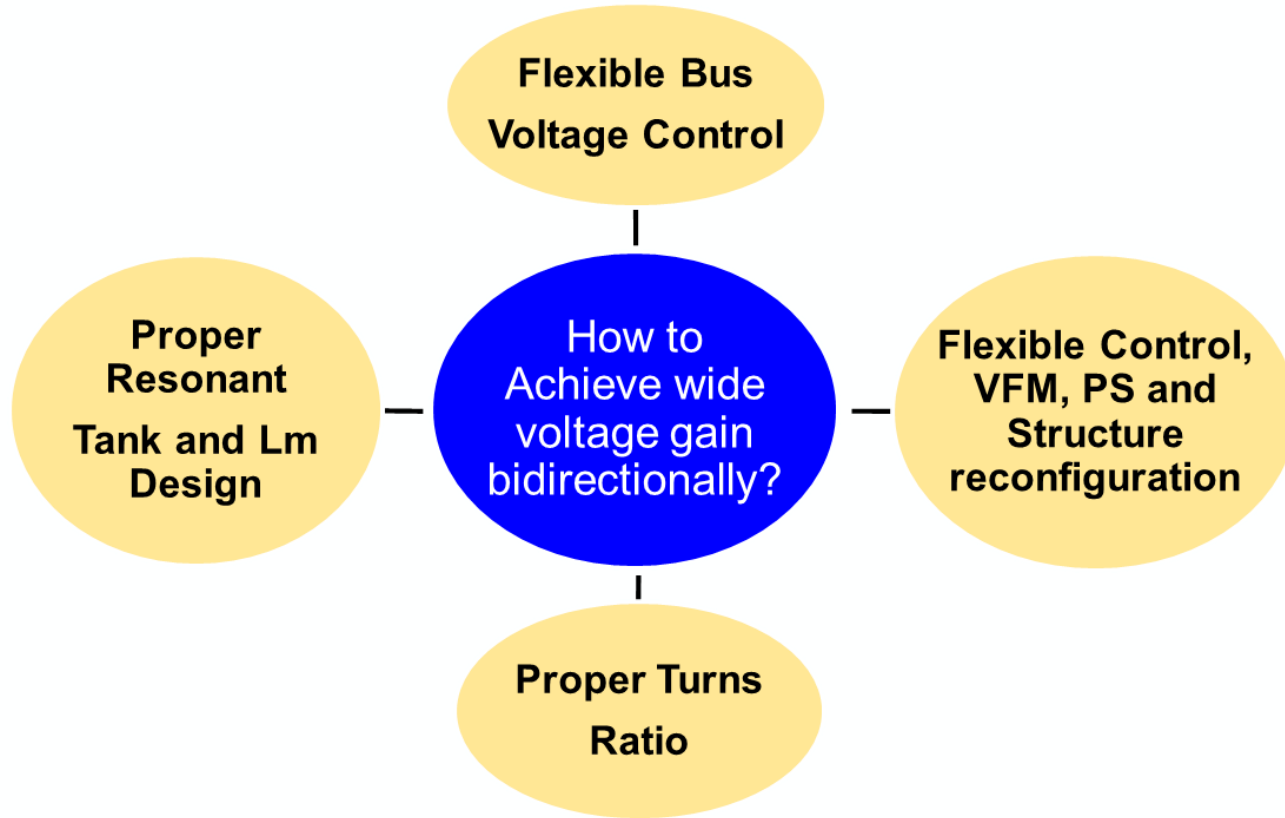
Description	3phase AC input Charging	1phase AC input Charging	Discharging Mode
Input Voltage	304Vac~456Vac	90Vac~277Vac	300Vdc-800Vdc
Output Voltage	200-800Vdc	200-800Vdc	220Vac
Rated Power	22kW 36A max	6.6kW	6.6kW
OBC peak Efficiency	>96%	>96%	>96%
DCDC peak Efficiency	>98.5%	>98.5%	>98.5%
DC Bus Voltage	650V-900V	380V-900V	360V-760V



# High Power Density, High Efficiency Design



# Wide Voltage Gain Design

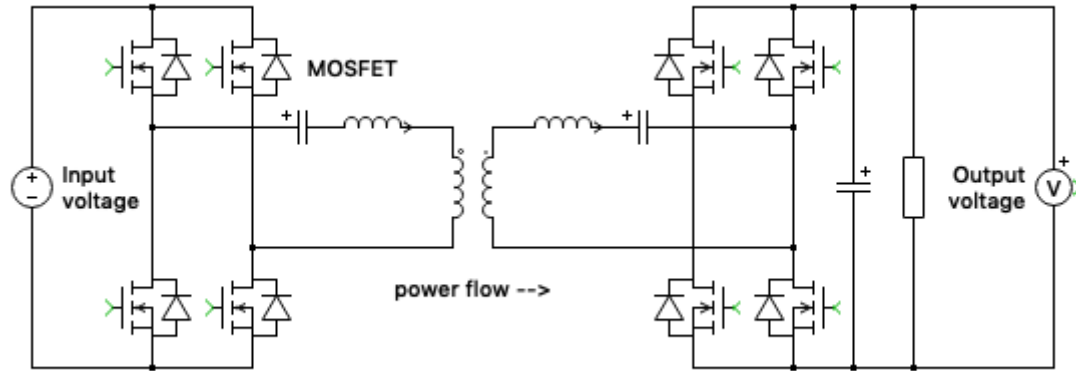


# Topology Selection

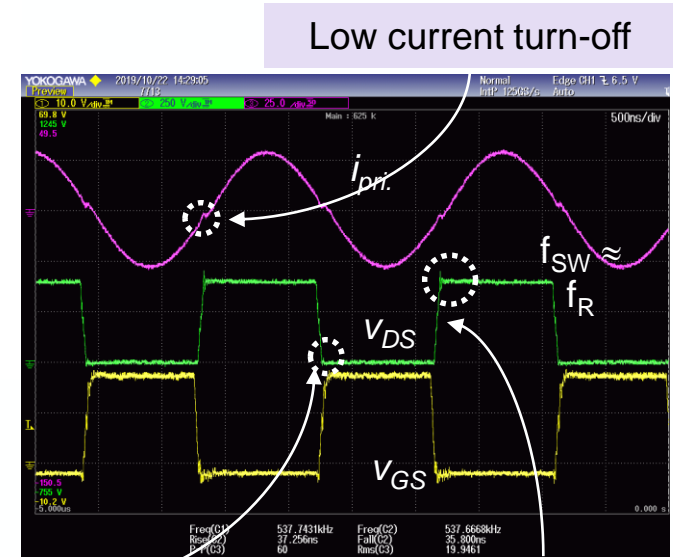
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# Candidate A for DCDC Converter

## Full Bridge CLLC Resonant Converter



- ✓ Zero Voltage Turn-On
- ✓ Low Current Turn-off → Low Switching Loss
- ✓ Bi-directional Operation
- ✓ Enable Flexible Control
- ✓ Enable high-frequency switching
- ✓ Low EMI

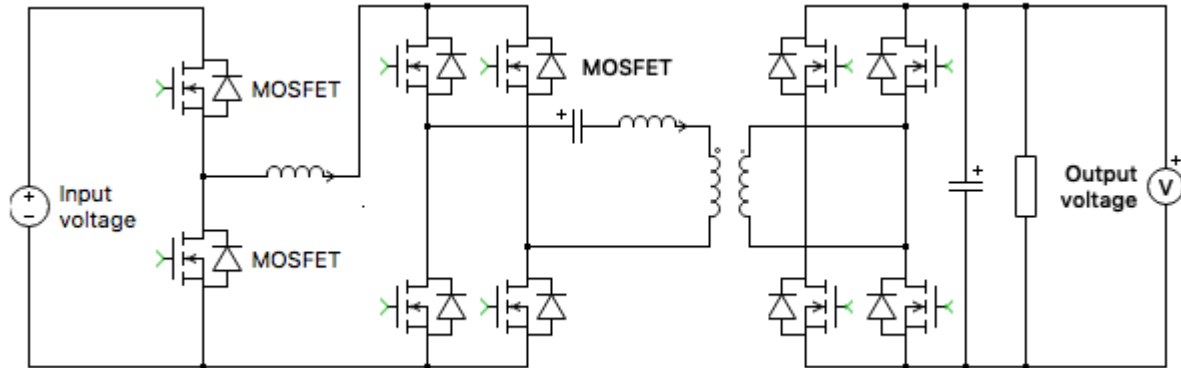


Zero voltage turn-on

Low voltage overshoot

# Candidate B for DCDC Converter

## Buck/Boost + Full Bridge DCX Resonant Converter



### Buck/Boost

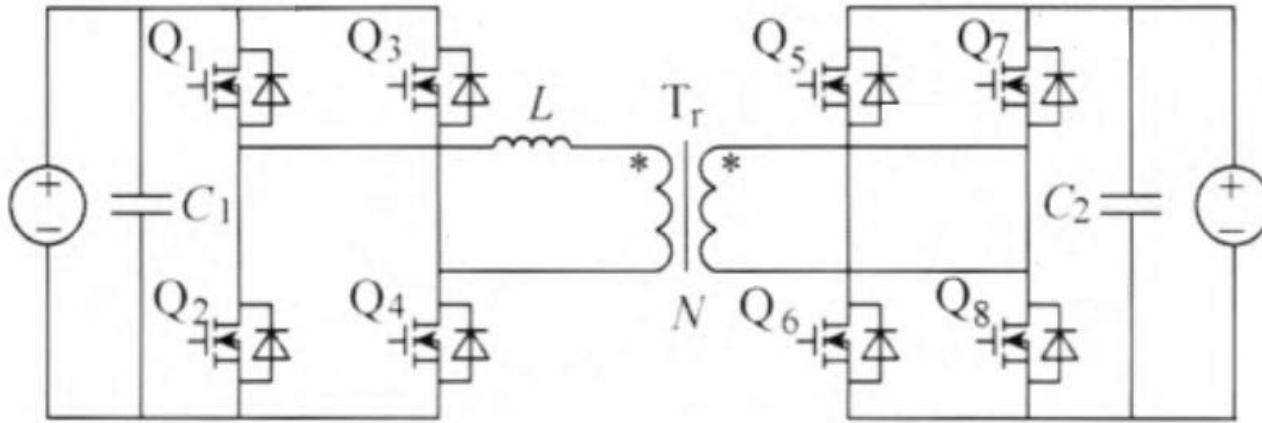
- ✓ Wide Voltage Gain Range by PWM Control
- ✓ Bi-directional Operation
- ✓ High Efficiency

### Full Bridge DCX Resonant Converter

- ✓ Zero Voltage Turn-On
- ✓ Low Current Turn-off → Low Switching Loss
- ✓ Bi-directional Operation
- ✓ Simple Fixed Frequency Control
- ✓ Enable high-frequency switching
- ✓ Low EMI

# Candidate C for DCDC Converter

## Dual Active Bridge Converter

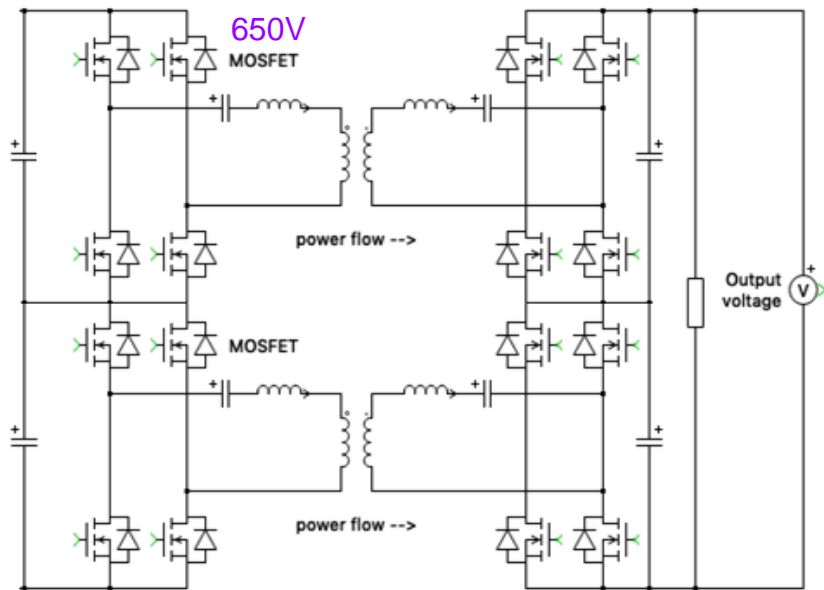


- ✓ Wide Voltage Gain Range
- ✓ Bi-directional Operation

- ✓ High Current Turn-off → high switching loss
- ✓ Lower Power density due to Limited switching frequency
- ✓ Limited Load Range for Soft-switching
- ✓ High di/t → EMI concern

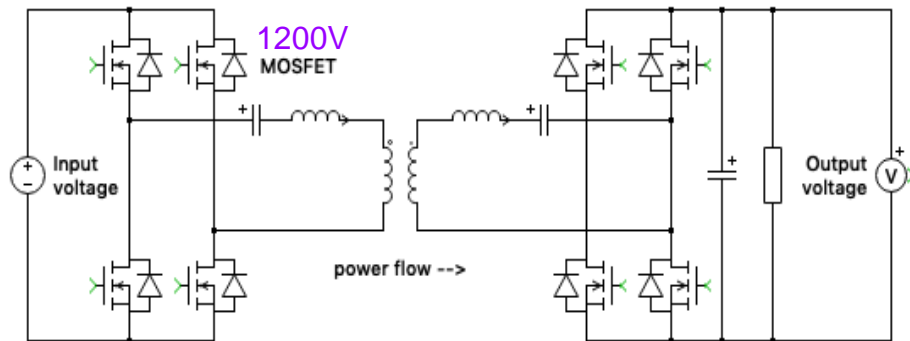
# Single Converter or Cascade

## Cascade Converter



**More part counts, higher conduction loss, Current sharing control required, Relay control at output, additional gate driver cost.**

## Single Two level Converter



**Lower part counts, higher power density and lower cost.**

- ✓ A single full bridge CLLC resonant converter is selected in this design.

# Power Components Selection

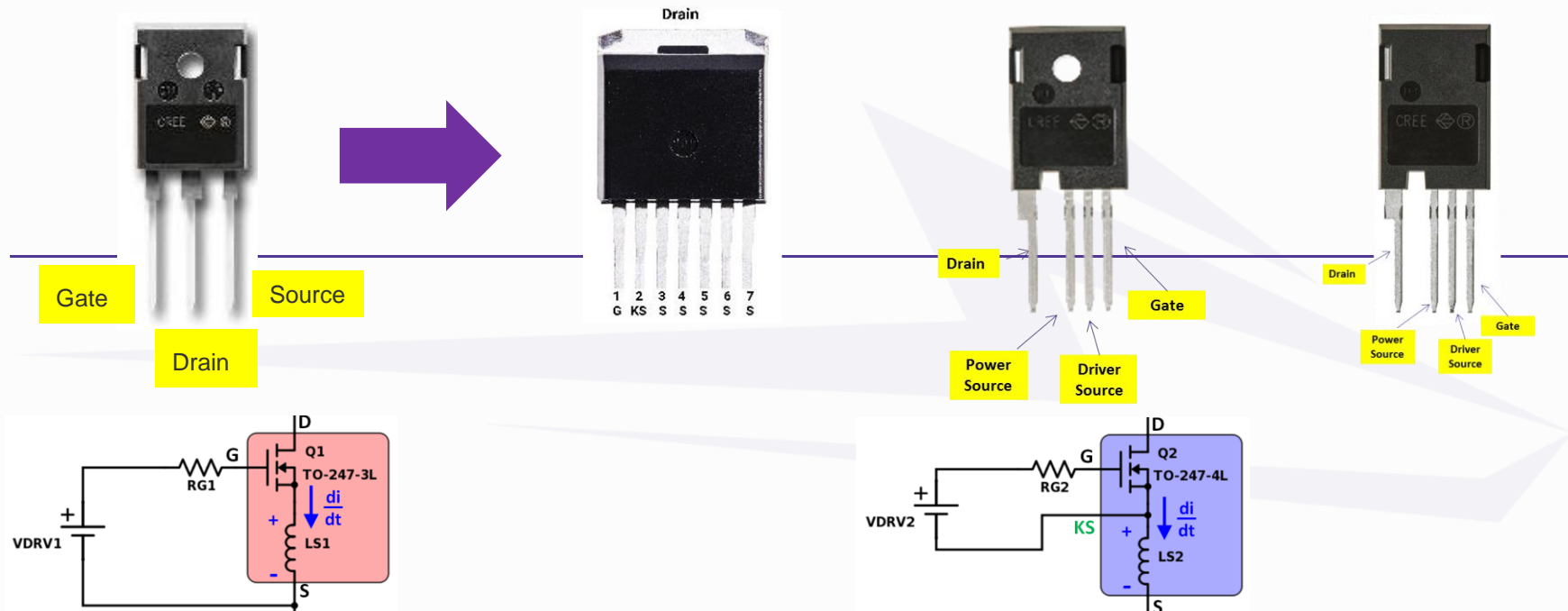
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# Why SiC?

- **Fast switching and low switching losses**
- **Less temperature dependence of  $R_{ds(on)}$  and low conduction loss at high temperature**
- **Smaller output capacitance, easier to achieve ZVS for CLLC resonant converter**
- **Low reverse recovery body diode enables reliability in case of hard-commutation**
  - ✓ **Enabling high-frequency switching**
  - ✓ **Increasing power density and reducing weight**
  - ✓ **High efficiency**
  - ✓ **Bi-directional operation**

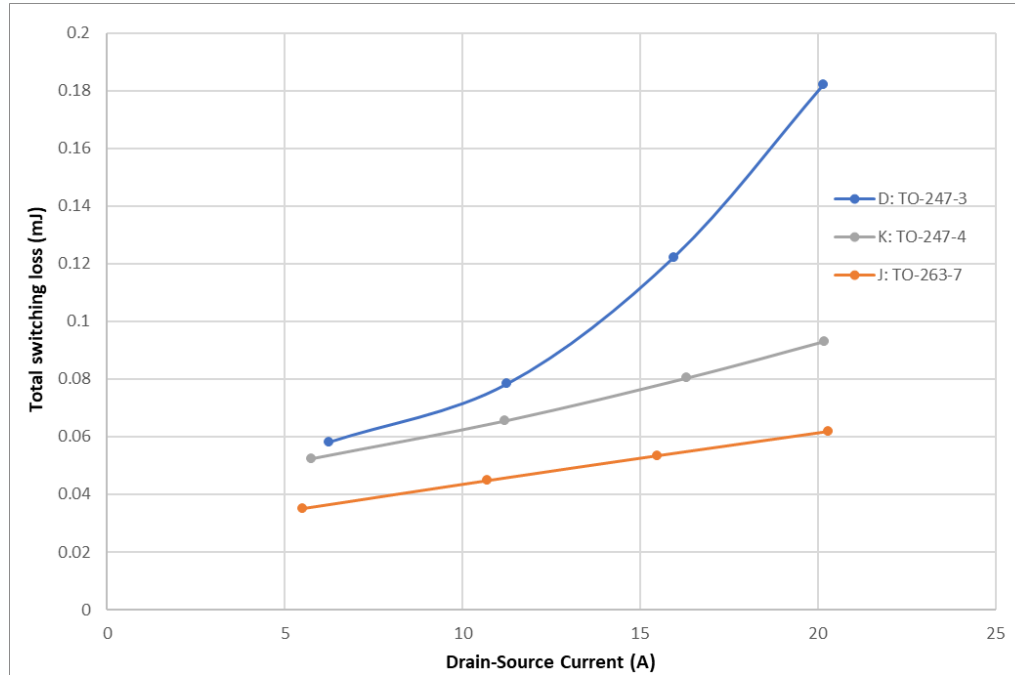
# Package Selection

## Recommended Optimized Packages with Kelvin Source Pin



# Switching Loss Comparison for Different Package

C3M0060060D/K/J @  $R_g=2.5\Omega$ ,  $V_{ds}=400V$



TO-247-3  
NO - Kelvin Pin  
2.6mm Creepage  
9.14nH Inductance



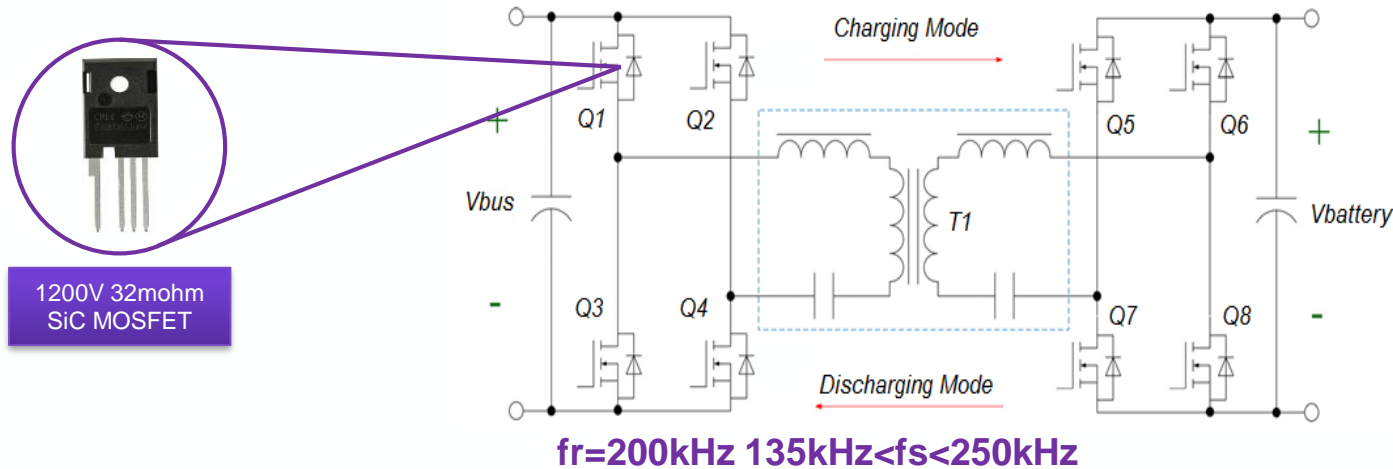
TO-247-4  
Kelvin Pin  
8mm Creepage  
7.36nH Inductance



TO-263-7  
Kelvin Pin  
7mm Creepage  
2.7nH Inductance

# Power Components Selection

The DC link voltage is up to 900V. Battery voltage is up to 800V.  
22.6A rms current for DC link side full bridge MOSFETs.  
28.5A rms current for battery side full bridge MOSFETs.



**C3M0032120K 1200V 32mohm SiC MOSFET is selected for both primary and secondary of CLLC converters based on electrical stress and thermal design.**

- ❑ Best figure of merit (FOM)
- ❑ New K-Source package reduces switching loss and reduce cross talk
- ❑ Easy to drive ( $V_{gs} = +15\text{V}$ )

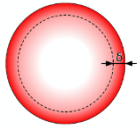
# Key Magnetics Design

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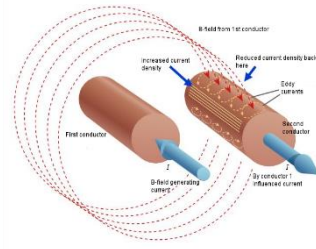
# Design Challenges

- ❑ High Power Density → High frequency operation
- ❑ High Efficiency → low power loss on both core and winding
- ❑ Balance between power loss and thermal management

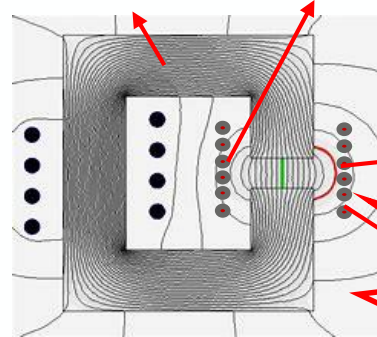
Skin Effect



Proximity Effect



Core Loss Thermal Management



Fringing Effect

Extra power loss due to Eddy Current

## Parameters and Performance Comparison– Power Choke

	APH	NPH	NPH-L	NPA	KAM
ui	60	60	60	60	60
Pv(100mT @50kHz)	250kW/m3	260kW/m3	200kW/m3	100kW/m3	200kW/m3
DC Bias (@100 Oe)	73%	61%	58%	55%	68%
Frequency Range	<200kHz	<200kHz	<200kHz	<300kHz	<300kHz
Vendor	AMOGREENTECH	POCO	POCO	POCO	KDM

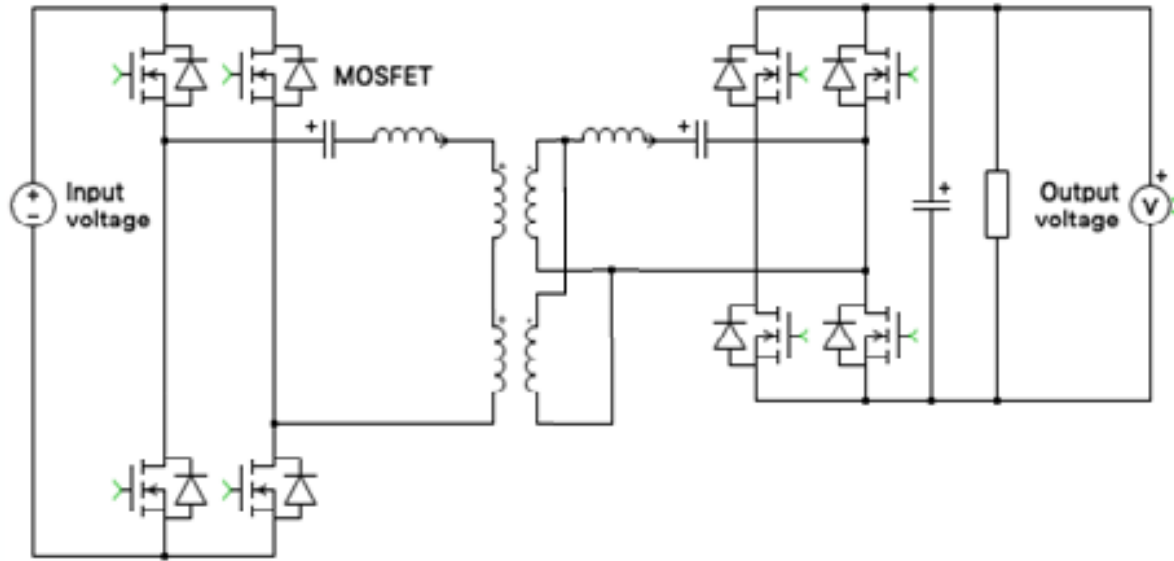
- ✓ KAM material is selected for PFC choke. It is a trade-off between core loss and DC bias.
- ✓ NPA material is selected for resonant chokes due to its lower core loss

## Parameters and Performance Comparison– Tx Core Material

	3C95	3C97	TPW33
ui	3000	3000	3300
Bmax	530mT@ 25 °C 410mT@ 100 °C	550mT@ 25 °C 430mT@ 100 °C	520mT@ 25 °C 410mT@ 100 °C
Pv(200mT/100kHz)	350kW/m3@ 25 °C 290kW/m3@ 100 °C	320kW/m3@ 60 °C 380kW/m3@ 140 °C	380kW/m3@ 25 °C 300kW/m3@ 100 °C
T_range optimized	25 °C-100 °C	50 °C-150 °C	25 °C-120 °C
Frequency Range	<500kHz	<500kHz	<500kHz
Vendor	Ferroxcube	Ferroxcube	TDG

- 3C97 is selected due to its wide temperature range for low power loss.
- However, 3C95 was used in samples build due to material shortage.

# Magnetics in the Converter



- Two transformers in serials at primary, in parallel at secondary. They are for good current sharing.
- Resonant tanks at both primary and secondary.

# Key Magnetics

- DCDC Transformer: PQ6562 Core

Contact info: Jinbo Cai, Sunlord, [jinbo\\_cai@sunlordinc.com](mailto:jinbo_cai@sunlordinc.com)

- Primary Resonant Choke: NPA158019 H18 Core

Contact info: Vivien Luo, POCO, [vivien\\_luo@pocomagnetic.com](mailto:vivien_luo@pocomagnetic.com)

- Secondary Resonant Choke: NPA158019 H12 Core

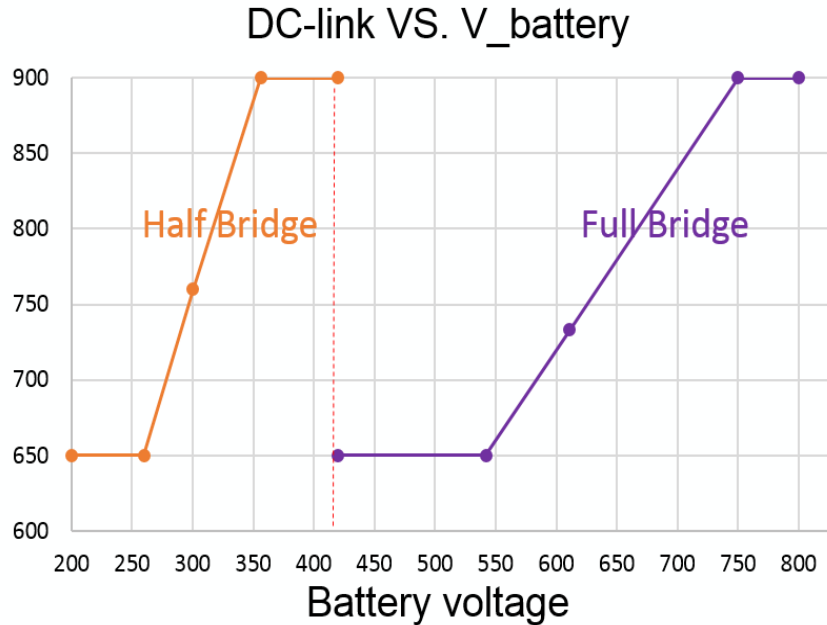
Contact info: Vivien Luo, POCO, [vivien\\_luo@pocomagnetic.com](mailto:vivien_luo@pocomagnetic.com)

# The Control of CLLC converter

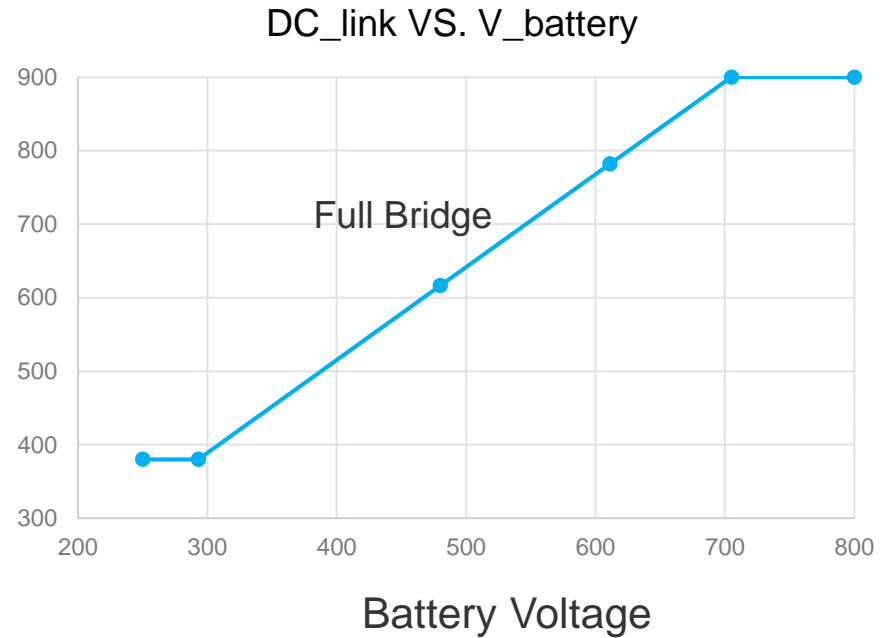
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# Flexible DC Link Voltage Control in Charging mode

3phase AC input 650V-900V



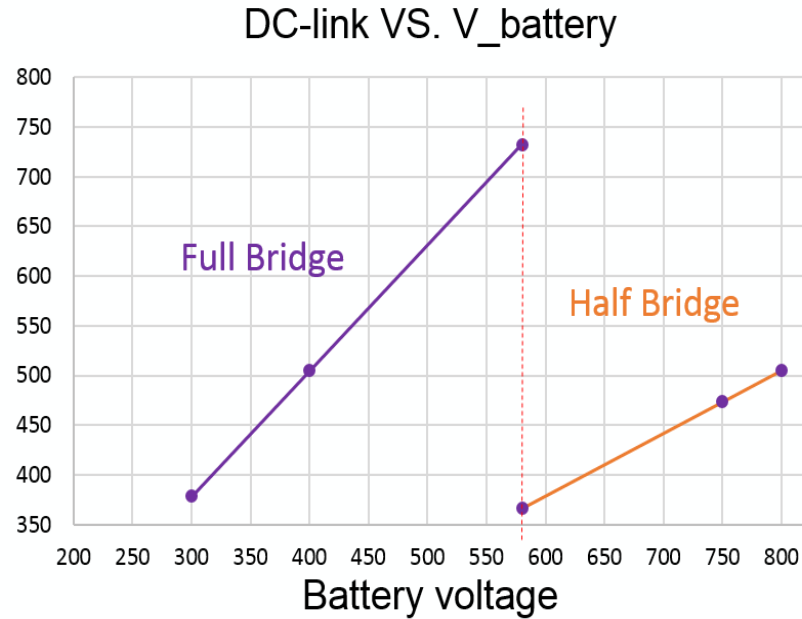
Single phase AC input 380V-900V



Wide range @ resonant frequency

# Flexible DC Link Voltage in Discharging mode

350V-750V



# Flexible Digital Control

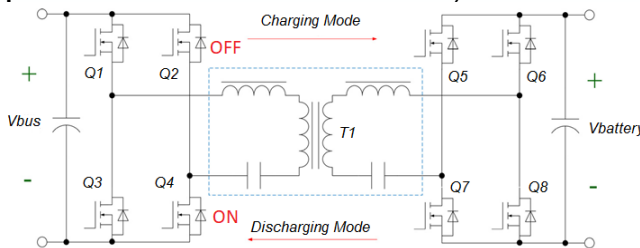
## Variable frequency control (PFM: Pulse Frequency Modulation)

Digital controller adjusts the switching frequency of the CLLC converter to provide the required voltage gain. The switching frequency range is 140kHz ~ 250kHz.

## Phase Shift Control

The upper limit of the switching frequency is 250kHz. At lower voltage output especially for light load, the required voltage gain of the CLLC is even lower than the gain @250kHz. The digital controller will adjust the phase of the PWM for one of the half bridges to further reduce the voltage gain of the converter.

If the converter operates in phase-shift mode, when the required gain becomes higher, the digital controller will adjust the phase to increase the gain. Once the phase shift reduces to zero, the PFM control scheme automatically take over the control.



## Structure Reconfiguration

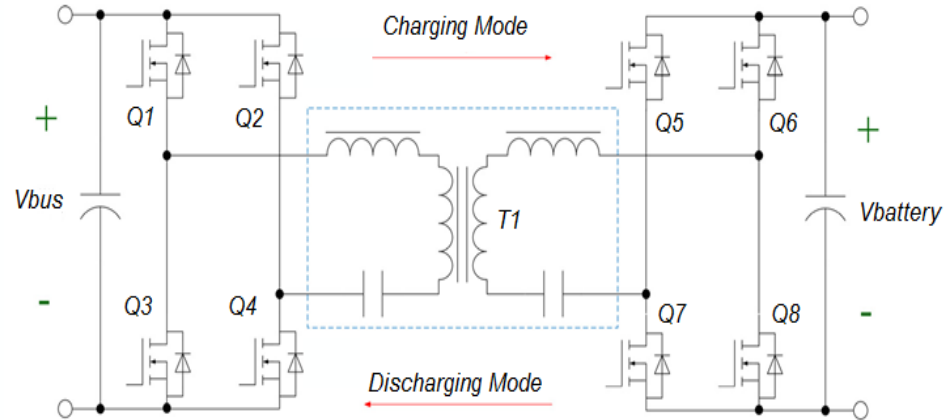
At extremely low voltage output, the full bridge CLLC can not have high efficiency @ the required voltage gain even in phase shift control mode @250kHz. Digital controller will reconfigure the converter to half bridge CLLC converter by turn-off Q2 and keep Q4 always on. It is to further reduce the gain and have a better efficiency in both charging and discharging mode.

# Adaptive SR Control

Adaptive SR is achieved by digital controller based on:

- Operation mode
- DC-link Voltage
- Output Voltage
- Output Current
- Switching frequency

Both turn-on and turn-off timing are tuned based on operation conditions in both charging and discharging mode.



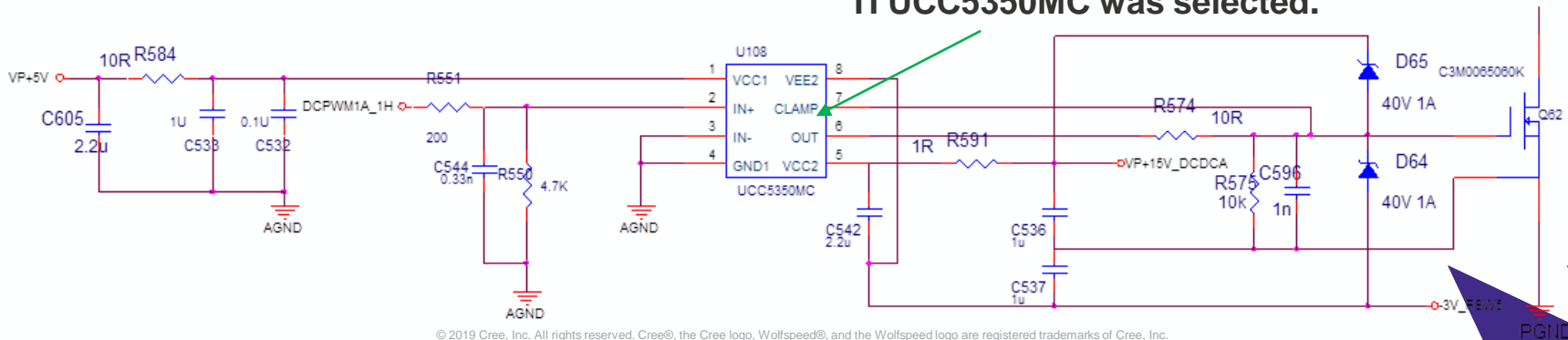
# Gate Driver and Bias Power Supply

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# Tips for SiC MOSFET Gate Driver Circuit

- CMTI ( $>100\text{KV}/\mu\text{s}$ )
- VIORM Maximum Working Insulation Voltage
- Driving capability
- Propagation delay time ( $\sim 50\text{nS}$ ) and channel mismatch time ( $\sim 10\text{nS}$ )
- Active miller clamp
- Gate supply voltage (+15V/-3V)
- Additional cap Gate to Source
- Gate voltage clamp if active clamp is not available in gate drive IC

**TI UCC5350MC was selected.**

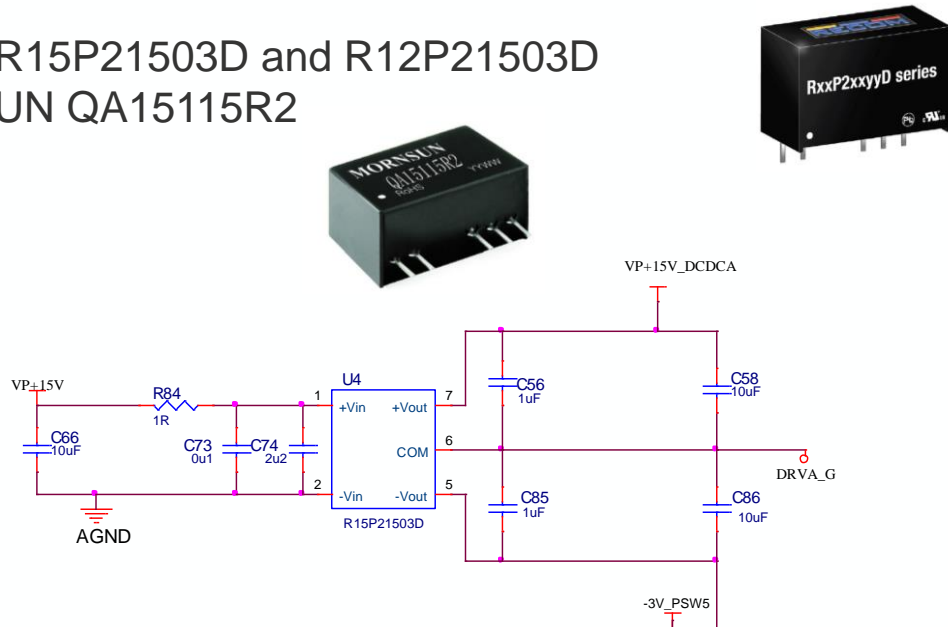


# How to Generate Bias Voltage?

## Dedicated +15V/-3V power supply

Wolfspeed has worked with partners (RECOM, MOURSUN) to make power modules

- RECOM R15P21503D and R12P21503D
- MOURSUN QA15115R2



Easy to use

# PCB Layout Considerations

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## Parasitic Caps of PCB

$$C = \epsilon_r S / 4\pi k d$$

$$1/4\pi k = 8.85 \times 10^{-12} \text{F/m}$$

$\epsilon_r$  of FR4  $\rightarrow \sim 4.3$

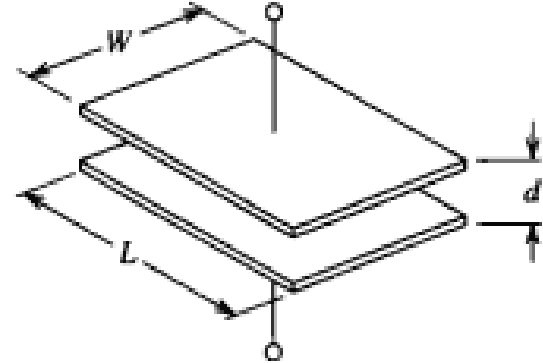
$$d = 0.0001 \text{m}$$

For 1 cm<sup>2</sup> PCB trace overlap:

$$C = 4.3 * 0.01 * 0.01 * 8.85 \times 10^{-12} / 0.0001 = 38 \text{pF}$$

$$P_c = 0.5 * C * f * V^2 = 0.304 \text{W for 400Vbus hard switching @ 100kHz}$$

- Short and small traces to reduce the coupling and parasitic capacitance



## Parasitic Inductance of PCB

$L = 0.2 \times l \times \left( \ln \frac{2 \times l}{w + t} + 0.2235 \times \frac{w + t}{l} + 0.5 \right)$  [nH]    l: Length(mm); w: Width(mm); t: thickness

Normally, the thickness of the PCB trace can be ignored. Then

$$L = 0.2 \times l \times \left( \ln \frac{2 \times l}{w} + 0.2235 \times \frac{w}{l} + 0.5 \right) \text{ [nH]}$$

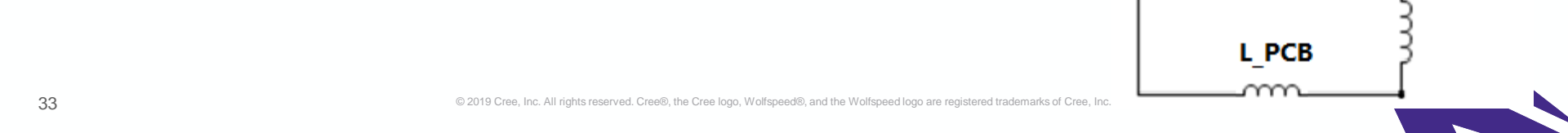
l: Length(mm); w: Width(mm)

For a 50mm length trace with 10 mm width, the PCB inductance:

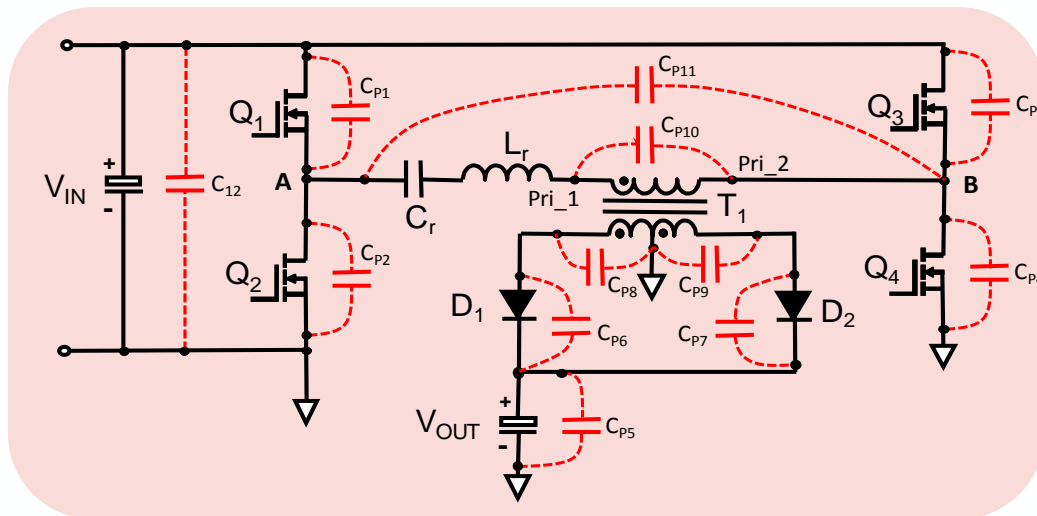
$$L = 0.2 \cdot 50 \cdot (\ln(2 \cdot 50 / 5) + 0.2235 \cdot 5 / 50 + 0.5) = 28.5 \text{ nH}$$

$\Delta V = L \cdot di/dt = 28.5 \cdot 50/20 = 71.25V$  voltage spike.

- Short trace reduces the voltage spike due to parasitic inductance.



# An Example for PCB Layout on Parasitic Capacitances

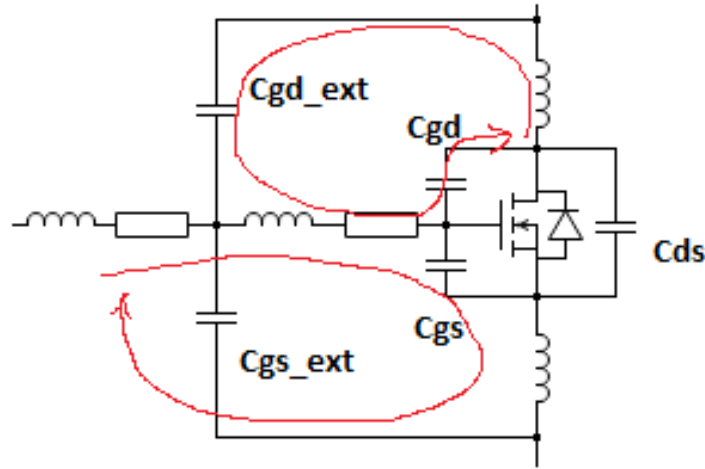


**Measured Parasitic Capacitances (Unit: pF)**

PCB Version	C <sub>P1</sub>	C <sub>P2</sub>	C <sub>P3</sub>	C <sub>P4</sub>	C <sub>P5</sub>	C <sub>P6</sub>	C <sub>P7</sub>	C <sub>P8</sub>	C <sub>P9</sub>	C <sub>P10</sub>	C <sub>P11</sub>	C <sub>P12</sub>	Efficiency (%)	Power Loss (W)
Ver. 1	315	390	343	420	4860	534	535	620	598	508	896	1385	95.71	141.57
Ver. 2	17	22	25	28	4731	528	516	589	575	11	13	308	96.50	115.50

Extra care for PCB layout crucial for maximizing efficiency!

# Enhanced Oscillation due to the external parasitic cap

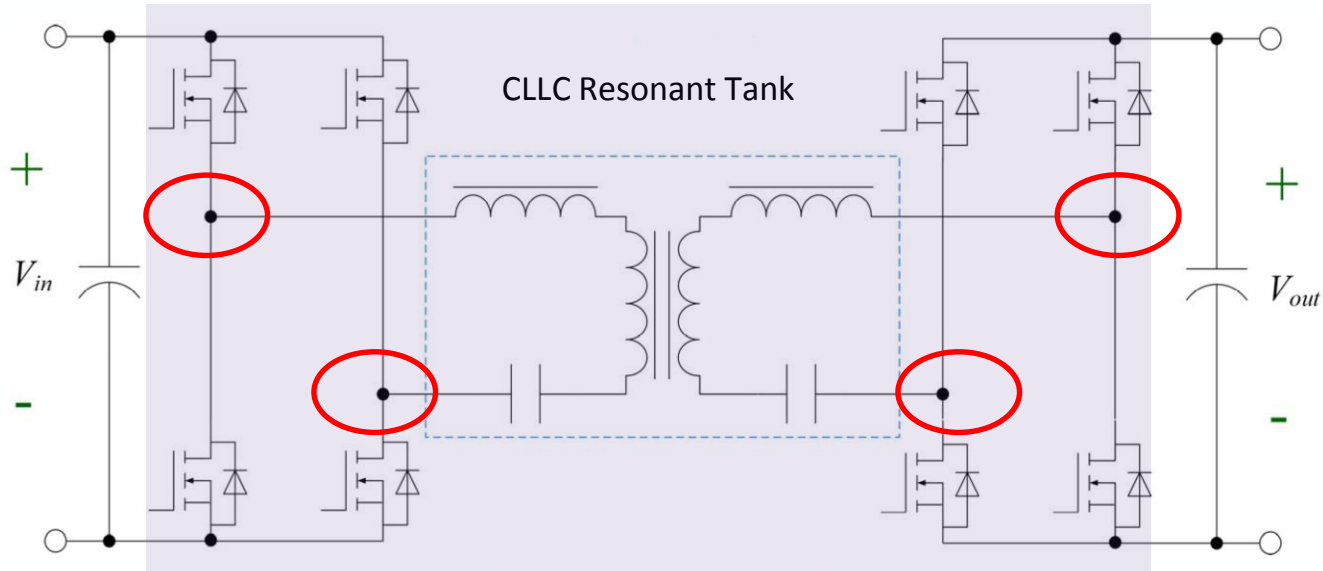


Parasitic cap by overlap between drain and Gate + Gate drive circuit.

$$I_D = (V_{GS} - V_{TH}) * g_{fs}$$

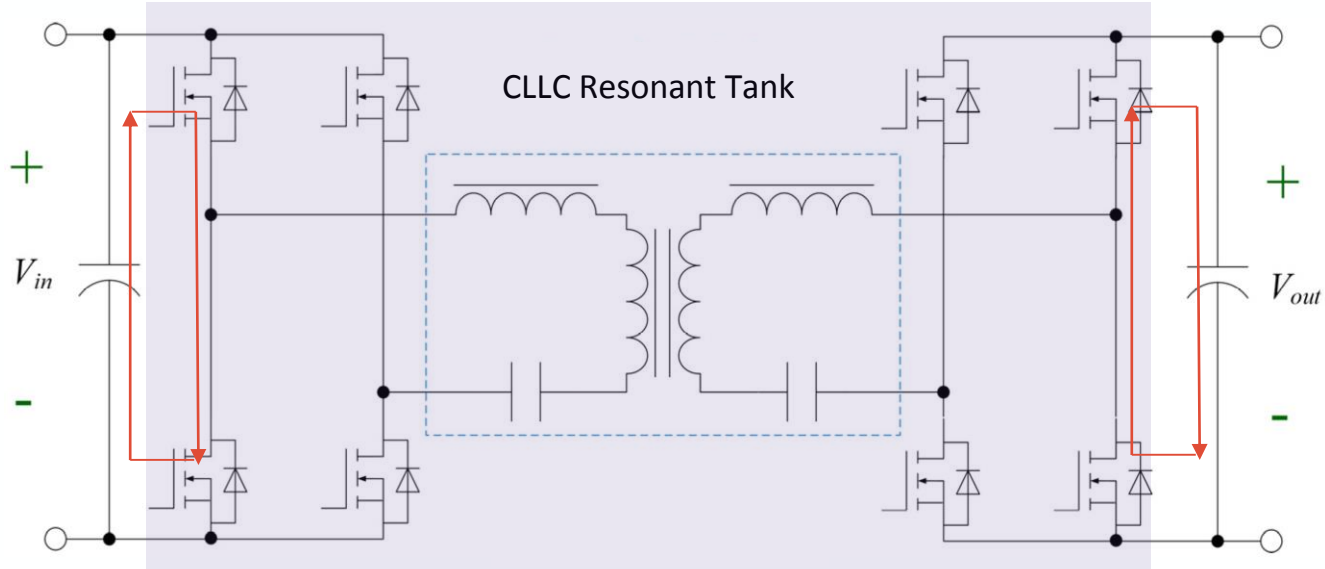
C<sub>gd\_ext</sub> can enhance the oscillation.

## High dv/dt trace/node



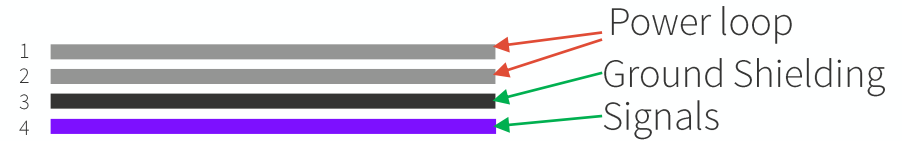
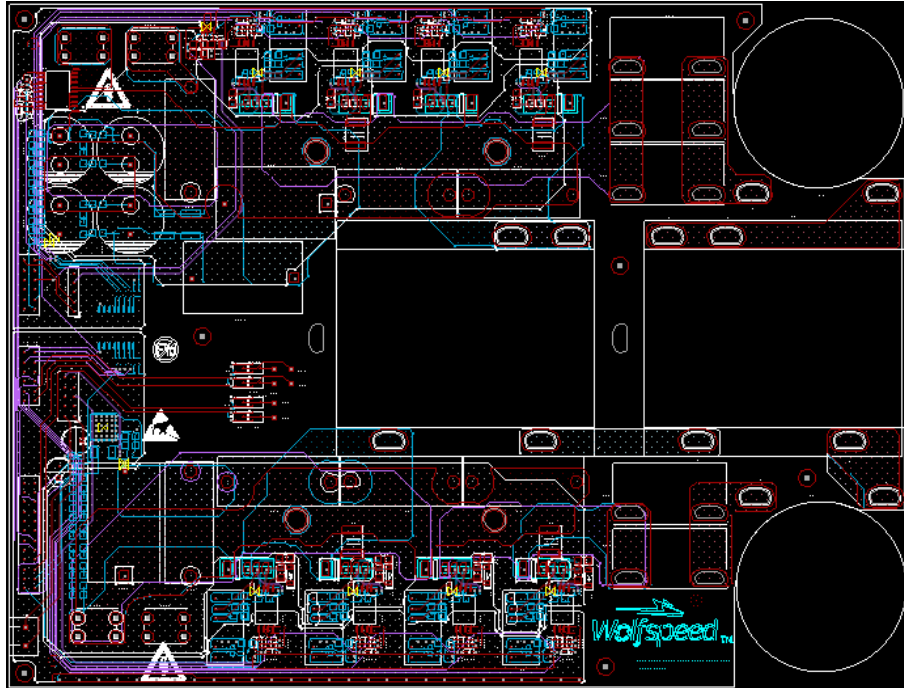
- Keep the sensitive signals far away from the high dv/dt trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as resonant choke, power transformer.
- Small pad size of Drain nodes to reduce the coupling and parasitic capacitance

## High di/dt loop



- Place ceramic or film caps as close as possible to minimize the high frequency di/dt loop.
- Proper PCB layout of the power components to minimize the high frequency di/dt loop.

# 4layers Power Board

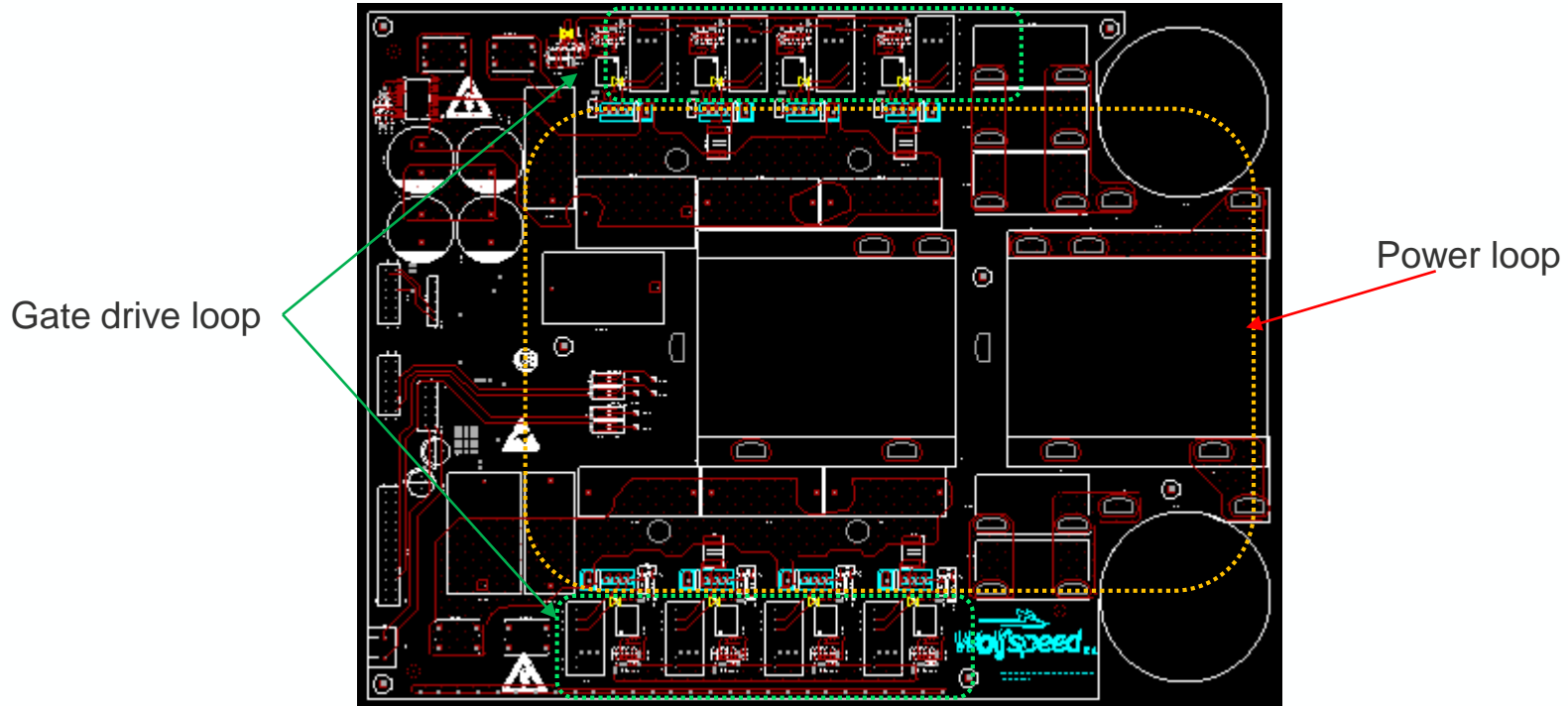


## Tips(for 4layers PCB):

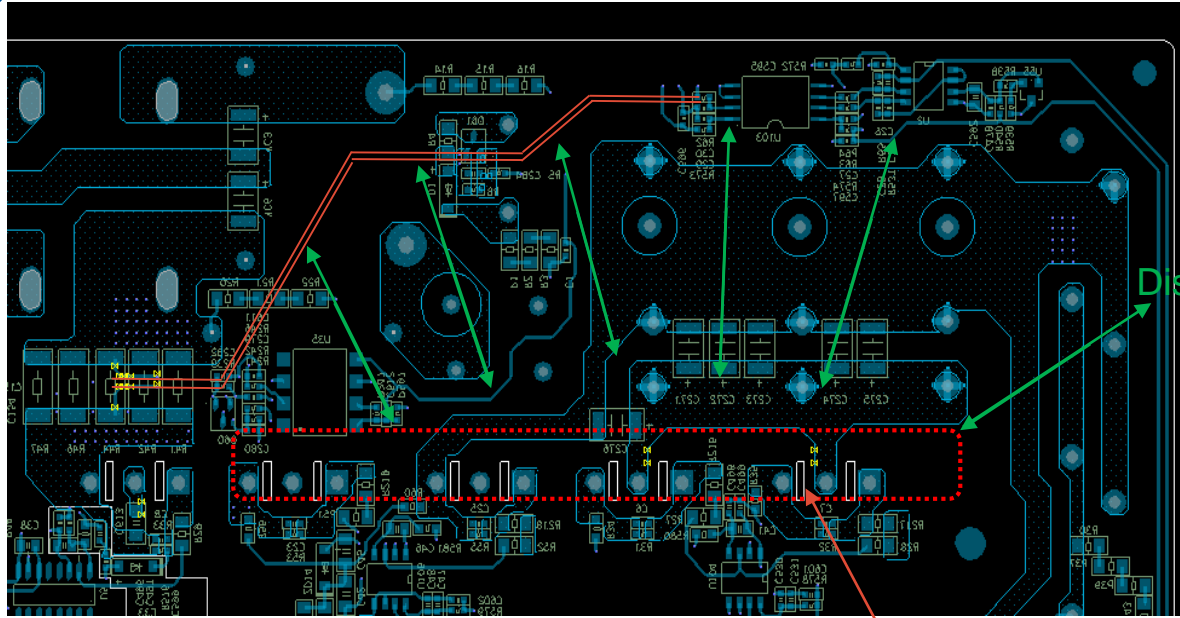
- No overlap between sensitive signals and the power loop.
- 3<sup>rd</sup> layer for GND.
- The ground layer acts as a shielding to cover the signal traces and gate drive circuit at the 4<sup>th</sup> layer.

# Components Placement

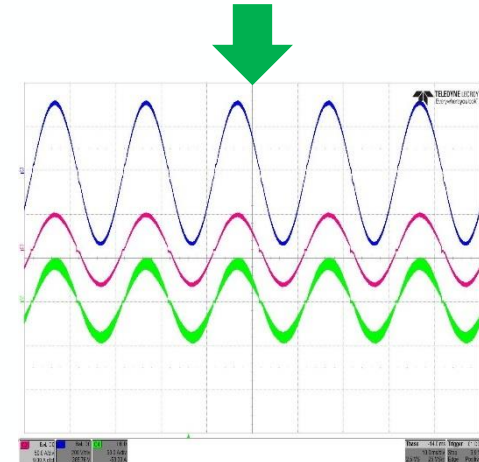
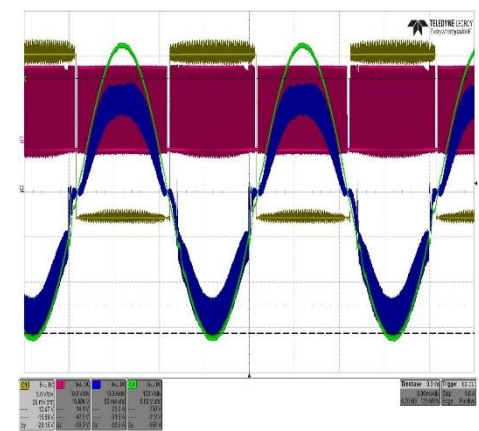
- Avoid overlap between Gate, Gate drive circuit, bias power supply for Gate drive and the drain of the MOSFET.



# High dv/dt trace/node



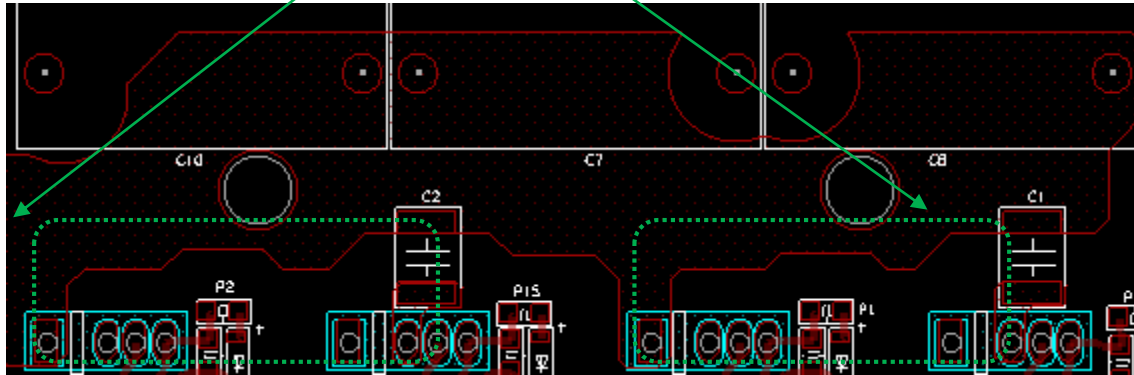
Distance!



- Keep the sensitive signals far away from the high  $dV/dt$  trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as PFC choke, DCDC power magnetics.
- Small pad size of Drain nodes to reduce the coupling and parasitic capacitance

# High di/dt loop

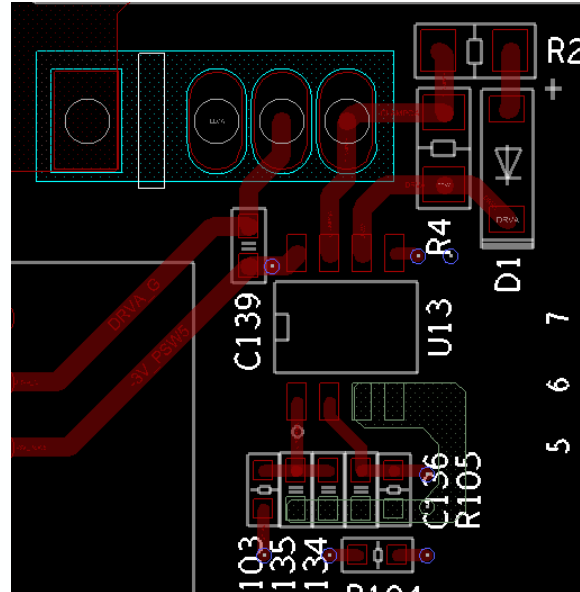
small di/dt loop



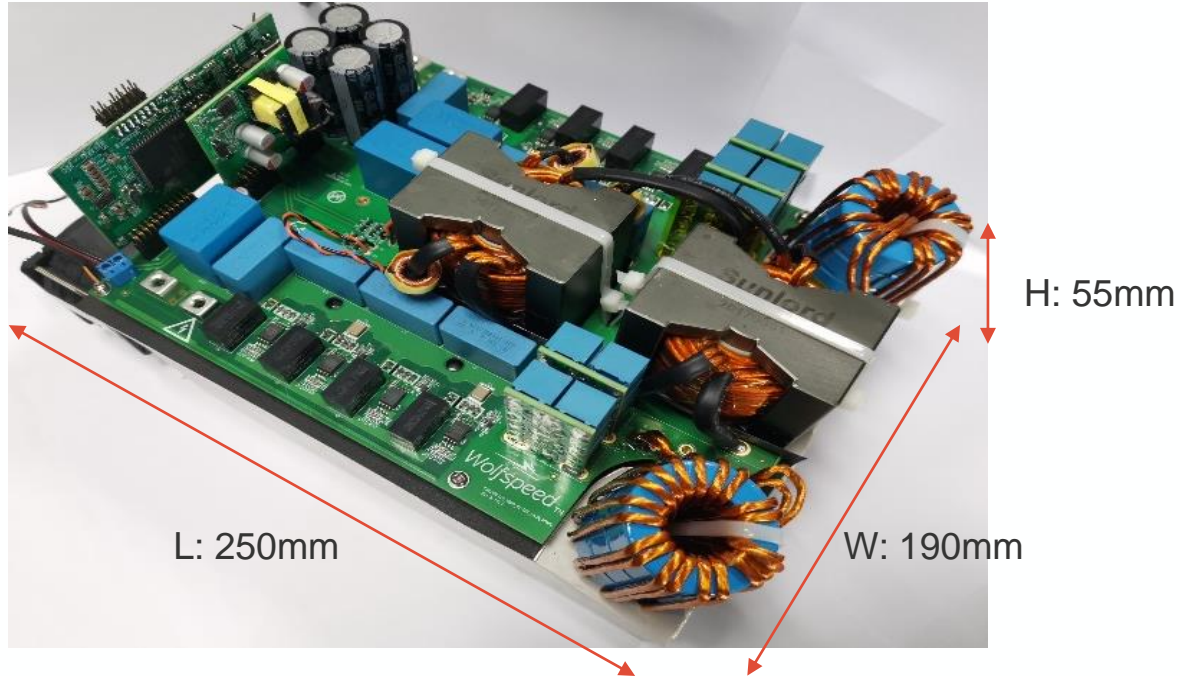
- Place ceramic or film caps as close as possible to minimize the high frequency di/dt loop.
- Proper PCB layout of the power components to minimize the high frequency di/dt loop.

# SiC MOSFET Gate Driver

- Minimized the loop of gate drive
- Minimized the loop of active miller clamp
- Separated gate source. Don't introduce parasitic inductance from power source loop
- Place the external Gate to Source cap as close as possible to the MOSFET



# Final PCB



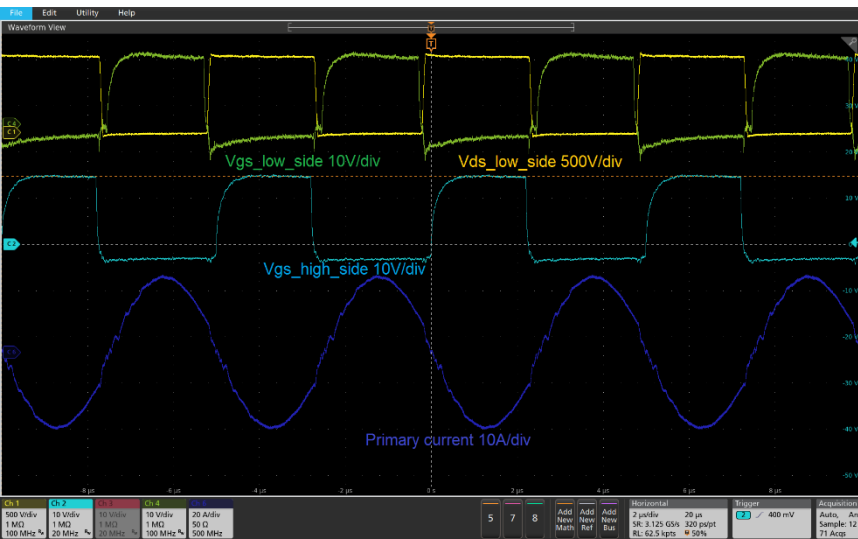
Power Density 8kW/L

# Test Results

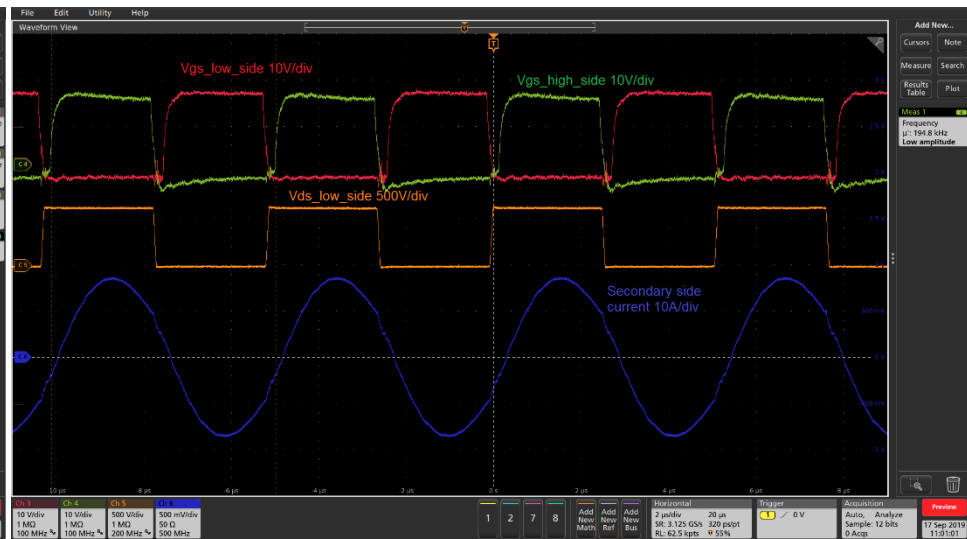
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# DCDC Waveforms

## Charging Mode



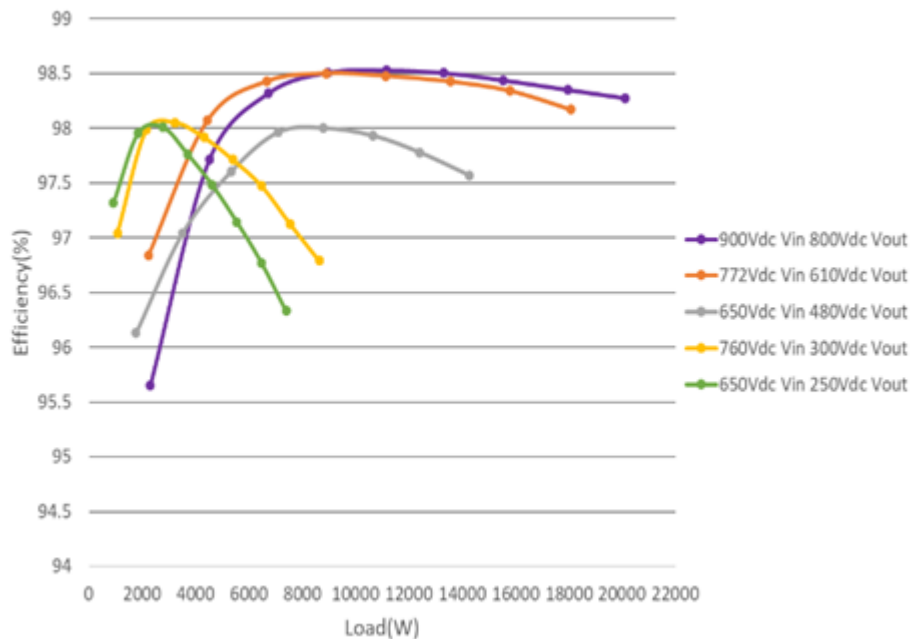
## Discharging Mode



# Efficiency Test Result

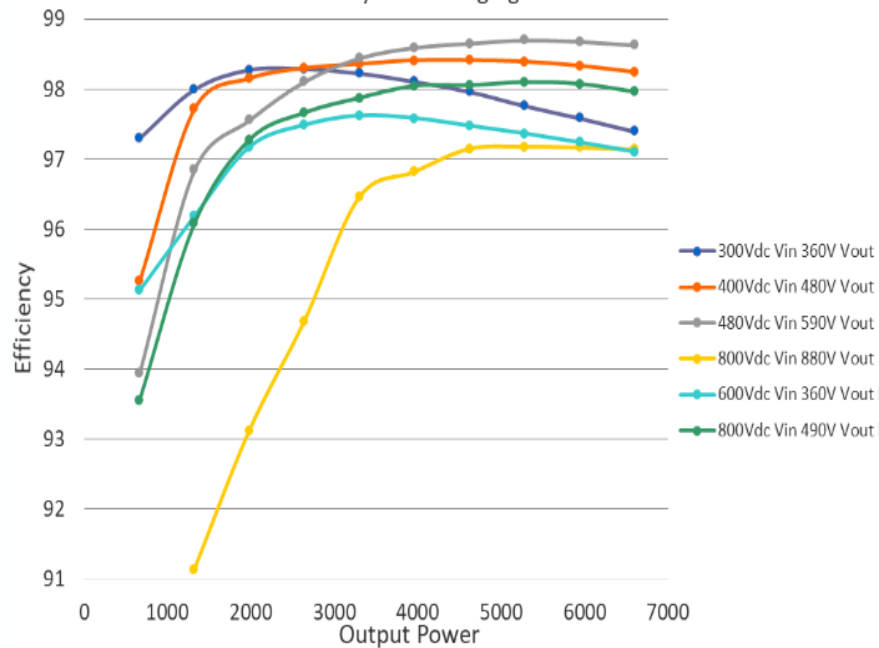
## Charging Mode

DCDC Efficiency in Charging mode



## Discharging Mode

DCDC Efficiency in Discharging Mode



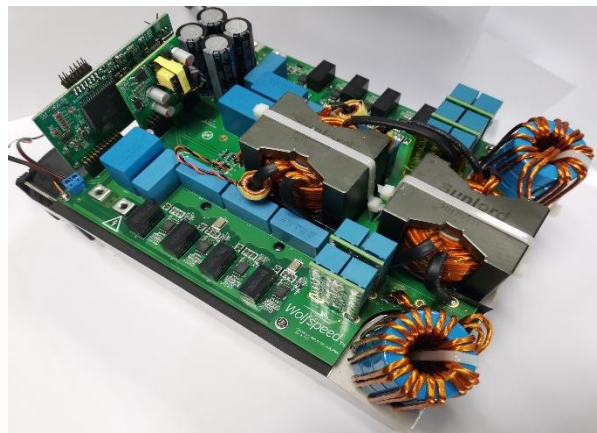
# Thermal Results

Description	Rth (j-c) (c/w)	Calculated Power Loss (watts)	Case Temp.	Calculated Junction Temp.	Max. Operating Junction Temp.	Comments
<b>Output = 611Vdc 22kW</b>						
<b>CLLC MOSFET</b>	0.45	32.5	87.6	102.2	175 °C	<b>PASS</b>
<b>CLLC SR MOSFET</b>	0.45	38	91.7	108.8	175 °C	<b>PASS</b>
<b>Output = 480Vdc 17.28kW</b>						
<b>CLLC MOSFET</b>	0.45	42	97.8	116.7	175 °C	<b>PASS</b>
<b>CLLC SR MOSFET</b>	0.45	38	92.1	109.2	175 °C	<b>PASS</b>

- $T_{\text{base plate}} = 65^{\circ}\text{C}$

# Summary

The C3M0032120K SiC MOSFET and the flexible control scheme enable high efficiency, high power density bi-directional OBC:



- ✓ High Power Density 8kW/L
- ✓ High Efficiency > 98.5% in charging and discharging mode
- ✓ Bi-directional Operation
- ✓ Support the DC link from both 3phase AC and single AC input
- ✓ Support 200Vdc-800Vdc wide battery voltage range

# Appendix

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# Topology Selection

## Dual Active Bridge Converter

## Full Bridge CLLC Resonant Converter

Advantages	Disadvantages	Advantages	Disadvantages
Fixed frequency Control	Lower efficiency due to high turn off current	Wide range ZVS → higher efficiency	To get a wide voltage gain range Hard to optimize the turns ratio, $L_m$ of transformer and $L_r$
Wide voltage gain range	Lower power density due to limited frequency	High frequency operation → Smaller Size, higher power density and lower cost	High frequency operation with high turnoff current in Buck mode → lower efficiency at lower $V_{out}$ .
	EMI concerns	ZVS operation, lower turn-off current → EMI friendly	Complex control for primary MOSFETS + adaptive control for SR MOSFET

✓ Full bridge CLLC resonant converter has better performance.

# Topology Selection

Buck/Boost +Full Bridge DCX Resonant Converter      Full Bridge CLLC Resonant Converter

Advantages	Disadvantages	Advantages	Disadvantages
Almost fixed frequency for DCX converter. → higher efficiency especially for low output voltage	Additional power stage and lower efficiency at system level	Single DCDC power stage → higher efficiency and higher power density	To get a wide voltage gain range Hard to optimize the turns ratio, $L_m$ of transformer and $L_r$
Easy to optimize Tx to get ZVS → lower magnetizing current, lower conduction & switching loss	More parts counts, → Larger Size, lower power density and higher cost	Lower parts counts, → Smaller Size, higher power density and lower cost	High frequency operation with high turnoff current in Buck mode → lower efficiency at lower $V_{out}$ .
Easy to control, both primary and SR MOSFET → higher reliability	Hard switching Buck/Boost converter → EMI concerns	ZVS operation, lower turn-off current → EMI friendly	Complex control for primary MOSFETS + adaptive control for SR MOSFET

- ✓ For high Power Density and lower cost, full bridge CLLC resonant converter is selected.

